Preliminary Results of Envelope Tracking Linearization of Solid-State RF Power Amplifiers for Efficient Superconducting Cavity Charging

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Summary

This paper presents the preliminary results of an experimental demonstration of envelope tracking (ET) technique applied on a kilowatt single-ended amplifier, which could be used to charge superconducting (SC) cavities at the European Spallation Source (ESS) at 352 MHz with a 5% duty cycle. The envelope tracking technique uses an optimal charging shaping function that minimizes the reflection power due to mismatch during the filling period. This is the first time that an optimal charging scheme is implemented using a solid-state based amplifier without degrading amplifier efficiency during operation.

1. Introduction

RF superconductive (SRF) cavities are becoming increasingly popular in modern particle accelerators, including the European Spallation Source (ESS), X-ray Free Electron Laser (XFEL), Linac Coherent Light Source (LCLS)-II, and the proposed International Linear Collider (ILC), due to their ability to achieve higher accelerating gradients with lower energy consumption. These cavities require charging to a nominal voltage before the beam can be injected, which is typically accomplished using high power RF sources such as Klystrons, Tetrodes, Inductive Output Tubes, and Solid-State Power Amplifiers (SSPAs). However, conventional step charging profiles lead to a large amount of reflected RF power during the initial filling period due to the cavities behaving as a mismatched load. To address this issue, previous work proposed shaping the profile of the applied RF power over time to minimize the total reflected power, demonstrating better performance compared to step charging. A time filling profile for the SC spoke cavities of the ESS is proposed, with the RF power source calculated to be approximately 400 kW with 5% duty cycle and 3.5 ms pulse width at a repetition rate of 14 Hz. Forward power and reflected power during cavity filling are depicted in Figure 1, the forward power and the reflected power profile are theoretically computed when applying both the step charging and optimal charging schemes. In the optimal filling scheme, the reflected power is minimized as low as 8 kW at start, as compared to 400 kW in step filling, then decreases exponentially as the filling continues [1].
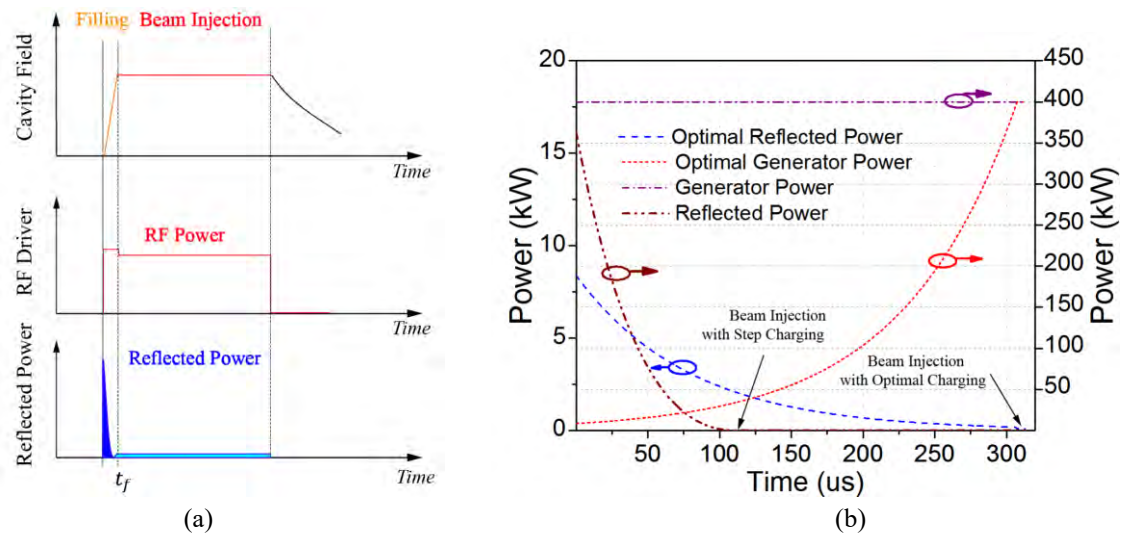

Figure 1: (a) Conceptual view of cavity field and RF timing for a superconducting cavity with step filling scheme, (b) generator and reflected power profiles in two schemes: step function (purple and brown traces) and optimal function (red and blue traces).

2. Architecture of the envelope tracking system and measurement setup

The envelope tracking power amplifier (ETPA) architecture typically consists of a linear power amplifier that is driven by a high-bandwidth modulator. The modulator generates a time-varying supply voltage that tracks the envelope of the input signal. This voltage is applied to the linear power amplifier to achieve high efficiency and minimize power dissipation. The ETPA can achieve high efficiency even when operating with high peak-to-average power ratios, which is often the case in

modern communication systems. See Figure 2 for the block diagram of the ETPA system, the measurement setup, and the practical implementation of the FPGA-based platform Xilinx Kintex-7 (XC7K325T-2FFG900C). The ADC and DAC boards 16-bit DAC34SH84EVM are connected to the KC-705 platform via high speed FMC adapter, allowing for a signal generation with an analog bandwidth up to 100 MHz. One DAC channel is used to create envelope shaping function for supply modulator while another DAC channel digitally generates RF pulsed signal. In the RF path, the signal is generated in digital base-band, then digitally up-converted to 352 MHz by digital up converter (DUC). The generated pulsed RF signal is amplified by a driver amplifier before feeding the 1kW SSPA module. This implementation could be applied with a high power amplifier such as the 10 kW demonstrator for ESS realized at 352 MHz [2]
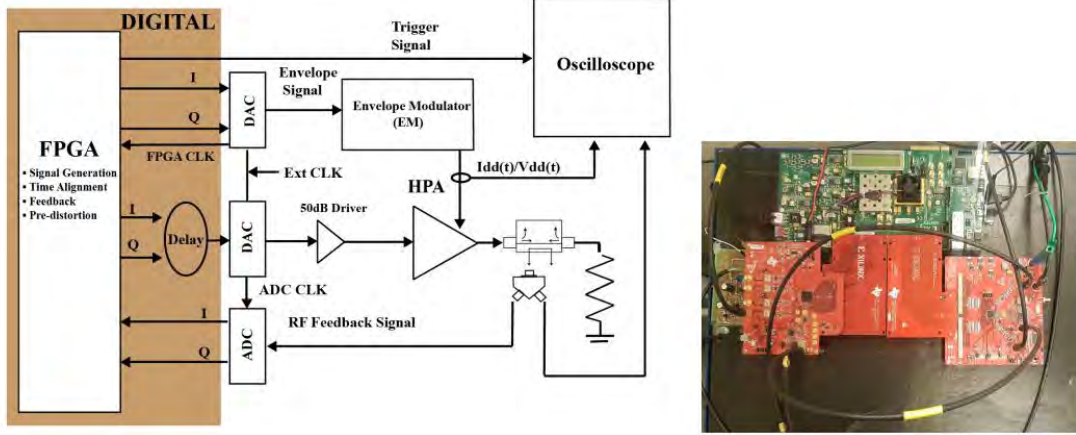

Figure 2: (a) Block diagram of the ETPA system and measurement setup, and (b) photograph of the FPGA-based platform.

3. Measurement results

The pre-distorter for the linearization of the SSPA module is working under signal modulation operation, and is implemented in open loop. The gain response of the SSPA module suffers from low drain voltage and low input power in the 250 μs to 275 μs region. This can be solved by adjusting the drain voltage and input power of the pre-distorter. The pre-distorter is chosen so that the region from 250 μs to 275 μs corresponds to inverted characteristics of SSPA module at fixed supply drain voltage. The region from 275 μs to 420 μs is then followed a triangle decay shape. The remaining region is kept constant, see Figure 3. The pre-distorted shaping function is given as $f(t)$ with modified values of K_1, K_2 and K_3 depending on the time region, see Eq. 1:

$$f(t) = \begin{cases} K1 * 10^{\frac{10 log_{10} \frac{\varepsilon (X_{rise}(t)*K2)^2}{K3*(sinh(2))^2} - 10}{20}} & \text{if } 0 \le t \le 300 \mu s \\ 1 & \text{if } 300 \mu s < t \le 3.5 ms \\ 0 & \text{elsewhere} \end{cases}$$
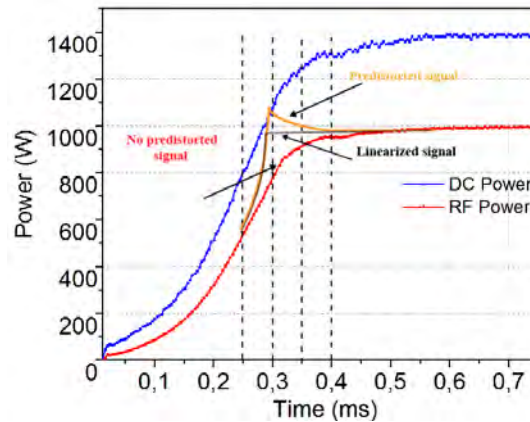

Figure 3: The targeted linear ET system is shown from 250 μs to 420 μs, the signal (the orange yellow trace) is pre-distorted allowing to optimize the linearity (the dashed black trace).

References

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[2] D. Dancila et al., "A compact 10 kW solid-state RF power amplifier at 352 MHz", IOP Conf. Series, 2017.